SOM 144

System-on-Module

Design Specification Rev. 1.0

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History

The SOM 144 specification and design guide has gone through revisions since its inception. To keep user's current with the latest version of the Advantech SOM 144 specifications and designs, this page lists the most recently printed revision of the SOM 144 specification and design guide. This revision history corresponds with the revision on the SOM 144 specifications and designs. The guide prints are ordered from oldest to newest.

Specification and Design Guide

Document No.	Date	Rev.	Changes Items
2006014410	31 May 2001	1.0	Initiation of SOM 144/ PCI Design Specification

Contents

CHAPTER 1

General Information

This chapter explains the concept of the SOM 144 (System-on-Module) module. It also gives the reasons why SOM 144 can give the most value and benefits to embedded system applications.

1.1 Overview

SOM 144 is a new form factor to speed up developing embedded systems. Simply put, it takes one SODIMM plus a front-end connector on a 2.5-inch-Hard-Drive-size PC board. Through the interface of the SODIMM transfer most of the common signals, such as PCI and USB interfaces for most of peripheral devices and IDE interface for Hard-Drive, CD-ROM, or Compact Flash. At the same time, special signals or other function requests go through the front-end connector.

Based on this specification, it is easier to develop a customer's solution board with an off the shelf SOM 144 module and reduce the time to market of your product. With the SODIMM socket and within 5 sec, a SOM 144 module is easy to install into or unload from customer's solution board.

This standard is a reference for board dimension and pinout of SOM 144 module. Different SOM 144 module may provide a different set of features. Please refer the datasheet or manual of your SOM 144 module for details or consult your supplier for supported features. SOM 144 modules are only interchangeable as long as they provide the same features. At this point, without changing customers' solution board, customers can upgrade the system module with higher performance CPU immediately. Some non-standard features like LCD display interface are not usable without external parts. To create a backplane or customer's solution board for SOM 144 module, it's highly recommended having experience with PCI device development. Furthermore, experience with signal integrity and timing for the layout of your solution board is recommended.

Please contact you supplier or Advantech for advice.

In addition to this document, the user should refer to the following industry standard specifications:

PCI Bus specification Rev 2.2
USB specification 1.1
ATX specification
AC97 Specification Revision 1.3, 2.0, and 2.1
HIROSE Catalog FX8 SERIES

CHAPTER 2

Connector Assignments and Descriptions

This chapter provides the pinout tables for the SOM 144 PCI interface, including the 144-pin SODIMM and recommended 80-pin frontend connector.

2.1 144-pin SODIMM (PCI/IDE/ Serial port /USB/AC97/KB/Mouse)

Table 2-1: Pinout of 144-pin SODIMM

Pin	Signal	Pin	Signal
1	GND	2	GND
3	VCC	4	VCC
5	IRQY	6	IRQX
7	IRQW	8	IRQZ
9	GND	10	PCIRST#
11	PCICLK1	12	GND
13	PCICLK2	14	PCICLK3
15	GND	16	GND
17	REQ#0	18	GNT#0
19	REQ#1	20	GNT#1
21	REQ#2	22	GNT#2
23	AD31	24	AD30
25	AD29	26	AD28
27	AD27	28	AD26
29	AD25	30	AD24
31	CBE#3	32	AD22
33	AD23	34	AD20
35	AD21	36	AD18
37	AD19	38	AD16
39	AD17	40	FRAME#
41	CBE#2	42	TRDY#
43	IRDY#	44	STOP#
45	DEVSEL#	46	PAR
47	LOCK#	48	AD15
49	GPERR#	50	AD14
51	SERR#	52	AD13
53	CBE#1	54	AD12
55	AD11	56	CBE#0
57	AD10	58	AD9
59	GND	60	GND
61	GND	62	GND
63	AD8	64	AD7
65	AD6	66	AD5
67	AD4	68	AD2
69	AD0	70	AD3
71	RESERVED	72	AD1

73	SERIRQ	74	RESERVED
75	HDRST#	76	PIDE_D8
77	PIDE_D7	78	PIDE_D9
79	PIDE_D6	80	PIDE_D10
81	PIDE_D5	82	PIDE_D11
83	PIDE_D4	84	PIDE_D12
85	PIDE_D3	86	PIDE_D13
87	PIDE_D2	88	PIDE_D14
89	PIDE_D1	90	PIDE_D15
91	PIDE_D0	92	PIDE_IOW#
93	PIDE_DRQ	94	PIDE_RDY
95	PIDE_IOR#	96	PIDE_A1
97	PIDE_AK#	98	RESERVED
99	PIDE_IRQ	100	PIDE_A2
101	PIDE_A0	102	PIDE_CS3#
103	PIDE_CS1#	104	BUZZER#
105	MSDAT	106	MSCLK
107	KBDAT	108	KBCLK
109	VCC	110	VCC
111	OVCR#	112	USB_EN#
113	USB01	114	ACSDTO
115	USB00	116	ACBITCLK
117	USB11	118	ACSDTI
119	USB10	120	ACSYNC
121	EXTRST#	122	ACRST#
123	DCD2#	124	DCD1#
125	DSR2#	126	DSR1#
127	RXD2	128	RXD1
129	RTS2#	130	RTS1#
131	TXD2	132	TXD1
133	CTS2#	134	CTS1#
135	DTR2#	136	DTR1#
137	RI2#	138	RI1#
139	VCC	140	VCC
141	VCC	142	VCC
143	GND	144	GND

2.2 Recommended 80-pin Front-end Connector (VGA/Ethernet/IrDA/Printer/FDD/ATX)

Table 2-2: Pinout of Recommended Front-end Connector

Pin	Signal	Pin	Signal
1	GND	2	RESERVED
3	GND	4	DDCK
5	DDAT	6	VSY
7	HSY	8	B
9	G	10	R
11	GND	12	STB#
13	AFD#	14	ERR#
15	INIT#	16	SLIN#
17	PD0	18	PD1
19	PD2	20	PD3
21	PD4	22	PD5
23	PD6	24	PD7
25	ACK#	26	BUSY#
27	PE	28	SLCT
29	GND	30	IRFRXH
31	IRCRX	32	IRRX
33	IRTX	34	GND
35	TXDN	36	TXDP
37	GND	38	RXDN
39	RXDP	40	GND
41	GND	42	5VSB
43	5VSB	44	5VSB
45	PME#	46	PWBT
47	PS_ON	48	CKRUN#
49	GND	50	GND
51	GND	52	RESERVED
53	RESERVED	54	RESERVED
55	RESERVED	56	RESERVED
57	RESERVED	58	RESERVED
59	RESERVED	60	RESERVED
61	RESERVED	62	RESERVED
63	RESERVED	64	RESERVED
65	RESERVED	66	RESERVED
67	RESERVED	68	RESERVED
69	GND	70	RESERVED
71	RESERVED	72	RESERVED
73	RESERVED	74	GND
75	SPEEDLED	76	ACTLED
77	GND	78	LILED
79	SDLED	80	GND

CHAPTER 3

Signal Description

This chapter details each signal defined in the SOM 144 Module.

3.1 144 pin SODIMM (PCI/IDE/ Serial port /USB/AC97/KB/Mouse)

GND	Ground.
VCC	+5V +/- 5% power supply.
RESERVED	Reserved pin.

3.1.1 PCI

All signals are 3.3 V level PCI signals. All pullups are integrated on the SOM 144 Module.

PCICLK1..3	PCI clock outputs for 3 external PCI devices.
REQ#0..2	Bus Request signals of 3 external PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter. Please refer the specification for your SOM 144 Module for used/ unused PCI Masters and shared PCI Masters with onboard devices.
GNT#0..2	Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.
AD0..31	PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBE#0..3	PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
PAR	Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBE#[3:0].
SERR#	System Error or PCI Clock RUN. The Northbridge asserts SERR# if parity errors are detected in DRAM.
GPERR#	Parity Error. For PCI operation per exception granted by PCI 2.1 specification.

LOCK# Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.

DEVSEL# Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.

TRDY# Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.

IRDY# Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.

STOP# Stop. This signal indicates the target is requesting the master to stop the current transaction.

FRAME# Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by Northbridge on behalf of CPU, or as an input during PCI master access.

PCIRST# PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.

IRQW, IRQX, IRQY, IRQZ
PCI interrupts from CPU-PCI bridge.

For further descriptions of PCI signals please refer to Chapter 4.

3.1.2 IDE

All required pullups are integrated on the SOM 144 Module. ESD and EMV protection devices need to be integrated on the backplane.

PIDE_D0..15 Primary/ Secondary IDE ATA Data Bus. These are the Data pins connected to Primary Channel.

PIDE_A0..2 IDE ATA Address Bus. These are the Address pins connected to Secondary Channel.

PIDE_CS1# Primary IDE Chip Select 1 for Channel 0. This command output pin enables the IDE device to watch the Read/Write Command.

PIDE_CS3# Primary IDE Chip Select 3 for Channel 1. This command output pin enables the IDE device to watch the Read/Write Command.

PIDE_DRQ IDE DMA Request for IDE Master. This is the input pin from the IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.

PIDED_AK# IDE DACK# for IDE Master. This is the output pin to grant the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.

PIDE_RDY IDE Ready. This is the input pin from the IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. In read cycle, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Busmaster to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Busmaster as DMA Ready (DDMARDY#).

PIDE_IOR#

IDE IOR# Command. This is the IOR# command output pin to notify the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different function. In read cycle, this pin is used by IDE Busmaster to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Busmaster will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.

PIDE_IOW# IDE IOW# Command. This is the IOW# command output pin to notify the IDE device that the available Write Data is already asserted by IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin is driven by IDE Busmaster to force IDE

device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.

PIDE_IRQ Interrupt signal.

HDRST# Low active hardware reset (RSTDRV inverted).

3.1.3 Serial Ports

All signals are TTL level signals. External drivers are necessary to convert the TTL signals to the desired physical interfaces, such as RS232, RS422,or RS485.

DCD1#, DCD2# This active low input for serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem.

DSR1#, DSR2# This active low input is for serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link.

RXD1, RXD2 Receiver serial data input.

RTS1#, RTS2# This active low output for serial port. Handshake signal notifies the modem that the UART is ready to transmit data.

TXD1, TXD2 Transmitter serial data output from Serial port.

CTS1#, CTS2# This active low input for serial ports . Handshake signal which notifies the UART that the modem is ready to receive data.

DTR1#, DTR2# Active low data terminal ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link.

RI1#, RI2# This active low input is for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem.

3.1.4 USB

All pullups are integrated on the SOM 144 Module. For ESD and

EMV protection please integrate the parts on you backplane.

USB00, USB01 Universal Serial Bus Port 0. These are the serial data pair for USB Port 0.

USB00 – negative signal, USB01 – positive signal

USB10, USB11 Universal Serial Bus Port 1. These are the serial data pair for USB Port 1.

USB10 – negative signal, USB11 – positive signal

USB_EN# USB Power Enable. This pin enables the power to a self-powered USB hub.

OVCR# Over current detect input. This pin is used to monitor the USB power over current. Pull with open-collector to GND if over-current is detected.

For further description of USB Bus please refer Chapter 7.

3.1.5 AC97

All signals are provided for directively connecting to a AC97 Codec or a AC97 compliant audio component on the solution boards for the audio funcion. Note that the codec must have SRC (sample rate conversion) support.

ACSDTO AC-Link Serial Data Output, CODEC Input Stream.

ACBITCLK AC-Link Bit Clock. 12.288 MHz Serial Data Clock. Daisy Chain Output Clock.

ACSDTI AC-Link Serial Data Input. CODEC Output Stream.

ACSYNC AC-Link Frame Sample Sync 48 kHz Fixed Rate.

ACRST# AC-Link Reset. CODEC Master H/W Reset.

3.1.6 PS/2 Keyboard/Mouse

All signals are not fused and without ESD and EMV protection circuitry. Protection devices will need to be incorporated onto the SOM 144 backplane.

MSDAT This is the bi-directional Mouse data signal.

MSCLK This is the Mouse clock signal.

KBDAT This is the bi-directional Keyboard data signal.

KBCLK This is the Keyboard clock signal.

3.1.7 Miscellaneous

SERIRQ Serial interrupt request. This pin is used to support the serial interrupt protocol. Please refer the manual of your SOM 144 Module for support of this signal.

BUZZER# This is the PC buzzer speaker output signal, connected to a speaker between output and VCC. Standard Speaker needs an External transistor. Max. sink current of this signal is 5mA.

EXTRST# External Reset.

3.2 Recommended front-end 80pin board to board connector (VGA/Ethernet/ IrDA/Printer/FDD/ATX)

GND Ground.

12V +12V +/- 5 % power supply

RESERVED Reserved pin.

3.2.1 VGA

All pullups are integrated on the SOM 144 Module. For ESD and EMV protection please integrate the parts on you backplane.

HSY Horizontal Sync: This output supplies the horizontal synchronization pulse to the monitor. It is normally not needed for flat panels.

VSY Vertical Sync: This output supplies the vertical synchronization pulse to the monitor. It is normally not needed for flat panels.

R, G, B Red, green and blue analog video output signals

for CRT displays.

DDCK, DDAT These two pins are functionally suitable for a DDC interface between the graphics controller chip and the CRT monitor.

3.2.2 Ethernet

All required pullups are integrated on the SOM 144 Module. ESD and EMV protection devices need to the please integrated on the backplane.

The SOM 144 Ethernet Interface is designed for use with a 1:1/ 1:1 external transformer.

Please refer to the electrical specification for further details.

TXDN, TXDP (Analog Twisted Pair)

Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface directly with an isolation transformer.

RXDN, RXDP (Analog Twisted Pair)

Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation.

ACTLED The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.

LILED The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.

SPEEDLED The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.

This LED is not supported by all SOM 144 boards.

All LED signals pulls a external LED with max. 5mA to GND.

3.2.3 IrDA

IrDA fuction of the SOM 144 Modules supports not only legacy IR IrDA 1.0 SIR, but also higher transmision protocals IrDA 1.1 MIR(1.152Mbps), and IrDA 1.1 FIR(4Mbps) and consumer IR.

IRTX, IRRX	Infrared transmit and receive pin.
IRFRXH	High speed IR receiving terminal
IRCRX	Consumer IR receiving terminal

3.2.4 LPT/FDD

All pullups needed for correct function are integrated on the SOM 144 Module. ESD and EMV protection devices need to be integrated onto the backplane. If the parallel port is used in parallel port mode, floppy disk support is not available via the parallel port. In case floppy support is need an external controller may be incorporated onto the backplane design.

STB#	LPT Mode:This active low pulse is used to strobe the printer data into the printer.
	FDD Mode: Not used.
AFD#	LPT Mode: This active low output causes the printer to automatically feed one line after each line is printed.
	FDD Mode:DRVDEN0.Drive Density Select bit 0.
ERR#	LPT Mode:This active low signal indicates an error situation at the printer.
	FDD Mode:HEAD#.Head Select. This output determines which disk drive head is active.
INIT#	LPT Mode:This active low signal is used to initiate the printer when low.
	FDD Mode:DIR#.Aoutput indicates the direction of the head step motor. Logic 1: outward motiion;

	Logic 0: inward motion.
PD0	LPT Mode:This bi-directional parallel data bus bit 0 is used to transfer information between the SOM 144 Module and peripherals. FDD Mode: INDEXJ.This input from the FDD is active low when the head is positioned over the beginnin of a track marked b an index hole.
PD1	LPT Mode:This bi-directional parallel data bus bit 1 is used to transfer information between the SOM 144 Module and peripherals. FDD Mode:TRAK0. Track 0. This input from the FDD is active low when the head is positioned over the outermost track.
PD2	LPT Mode:This bi-directional parallel data bus bit 2 is used to transfer information between the SOM 144 Module and peripherals. FDD Mode:WP#. Write Protected. This active low input from the FDD indicated that the diskette is write-protected.
PD3	LPT Mode:This bi-directional parallel data bus bit 3 is used to transfer information between the SOM 144 Module and peripherals. FDD Mode:RDATA#. Read Data . The input signal from FDD.
PD4	LPT Mode:This bi-directional parallel data bus bit 4 is used to transfer information between the SOM 144 Module and peripherals. FDD Mode:DSKCH#. Diskette Change. This active low signal at power on and when the diskette is removed.
PD5..7	LPT Mode:This bi-directional parallel data bus bit 5..7 are used to transfer information between the SOM 144 Module and peripherals. FDD Mode: Not used.

SLIN# LPT Mode:This active low signal for the SOM 144 Module to select the printer.

FDD Mode:STEP#. Step Output Pulses. This active low output produces a pulse to move the head to another track.

ACK# LPT Mode:This active low output from the printer indicates it has received the data and is ready to receive new data.

FDD Mode:DSB#. Drive Select B. When set to 0, this output selects FDD B.

BUSY LPT Mode:This is active high iutput for SOM 144 Module. This signal indicates the printer is busy and not ready to receive new data.

FDD Mode:MOB#. Moter B On. When set to 0, this output enables FDD B.

PE LPT Mode:This signal indicates that the printer is out of paper.

FDD Mode:WD#. Write Data. This active low open drain for the SOM 144 Module writes precompensation serial data to the selected FDD.

SLCT LPT Mode:This active high output from the printer indicates that it has power on.

FDD Mode:WE#.Write Eable. An open drain output for the SOM 144 Module.

3.2.5 Miscellaneous

5VSB Power supply input for the internal suspend circuit. Connect to 5V Stand by power if available from ATX power supply.

PS_ON When removing all circuit power except the internal suspend circuit, PS_ON will become active high to disable all the circuits except the internal suspend circuit. You have to connect to PS-ON of your ATX power supply.

PWBT	Power Button Input. Connect with switch or open collector driver to GND for ATX power button function.
PME#	Power management event. It describes wake-up function in PCI bus.
CKRUN#	It is used by the system to pause or slowdown the PCI Clock signal. When the CKRUN# signal is not used, this pin should be connected to an external pull-down resistor.
SDLED	The SSD LED indicates the status of the SSD on the SOM 144 module

CHAPTER 4

Mechanical Characteristics

4.1 Mechanical Characteristics

4.1.1 Dimensions of SOM 144 Module

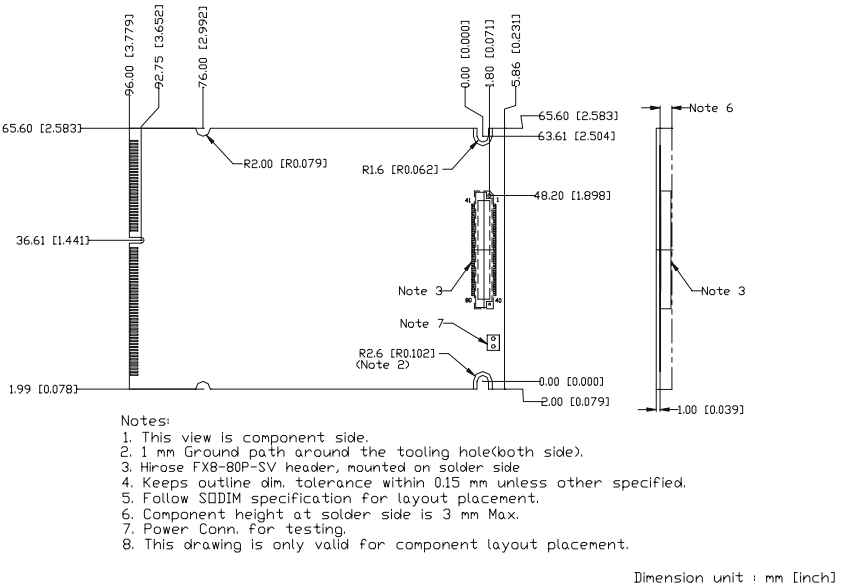

Figure 4-1: Dimensions of SOM 144' Module

4.1.2 SOM 144 Solution Board Layout

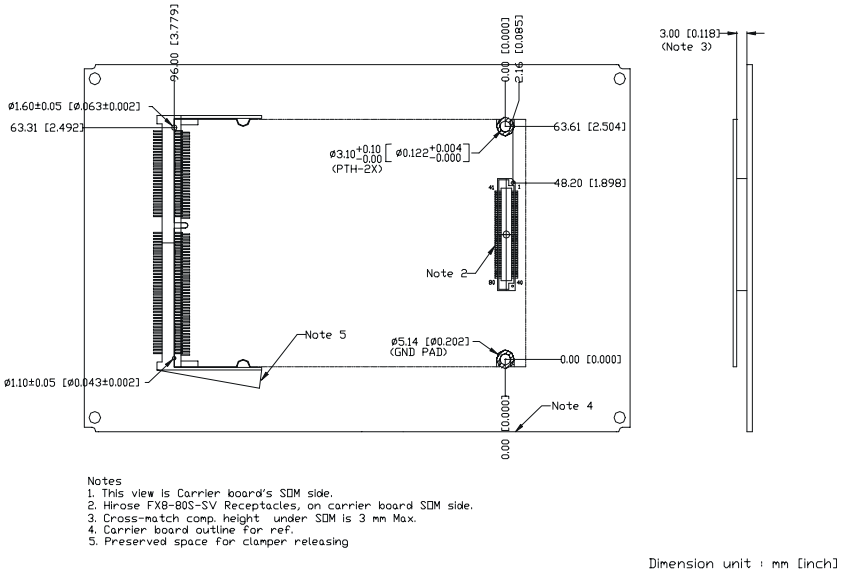

Figure 4-2: SOM 144 Solution Board Layout

4.1.3 Recommand Component Suppliers

At least 3.0 mm height is needed between the carrier board's surface and the bottom of SOM 144 Modules.Therefore, SODIMM socket must meet this requirement and so as the recommended board -to-board connector. Some suggested suppliers are listed below.

Componet	Model No.	Supplier
Recommended 80-pin front-end connectors	FX8C-80P-SV Header FX8C-80S-SV Receptacle	Hirose
SODIMM socket	C-390112	AMP

4.1.4 SODIMM Layout

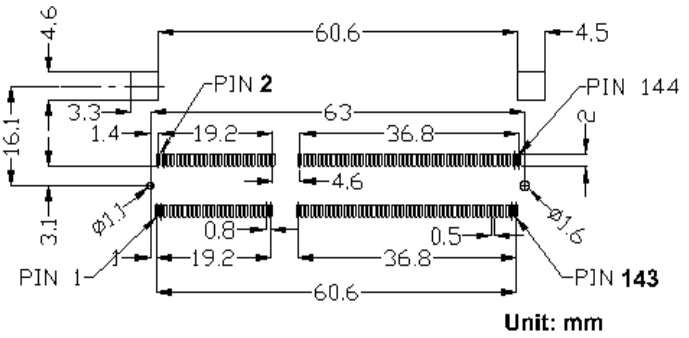

Figure 4-3: 144-pin SODIMM Layout

4.1.5 SOM 144 Module Installation

1. Plug the SOM 144 module into the solution board's SODIMM socket
2. Connet the front-end connector to the solution board
3. Screw the SOM 144 Module and the solution board together

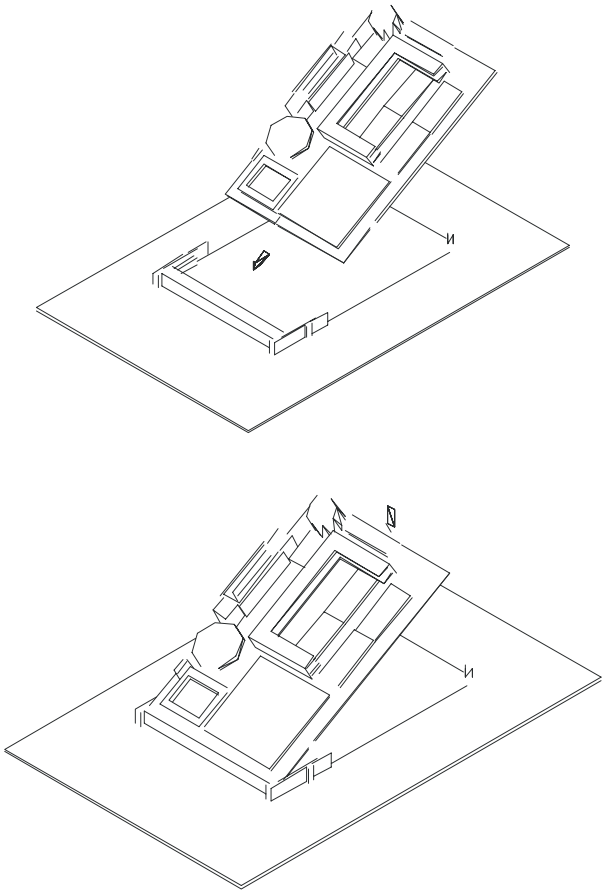

Figure 4-4: SOM 144 Module Installation

4.1.6 SOM 144 Module Removal

1. Unscrew two screws
2. Bend out the positioning holders of the SODIMM socket and release the SOM 144 Module
3. Unplug the SOM 144 Module from the socket

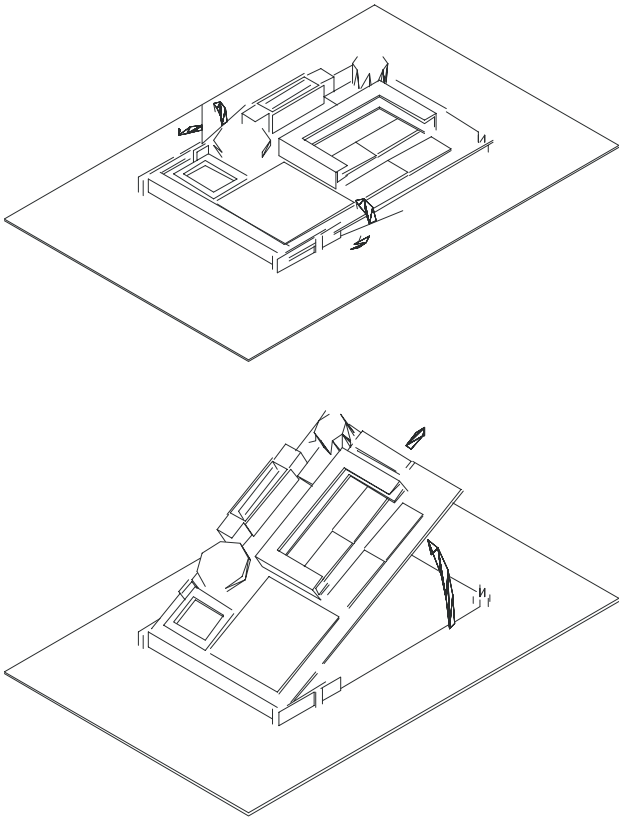

Figure 4-5: SOM 144 Module Removal

CHAPTER 5

Electrical Characteristics

5.1 PCI Bus

5.1.1 IDSEL mapping

AD line	Description
AD21	SOM 144 Backplane device # 1
AD22	SOM 144 Backplane device # 2
AD23	SOM 144 Backplane device # 3

5.1.2 Interrupt-Routing

Following interrupt routing on the backplane is recommended for proper BIOS support:

Device Number on SOM 144 Solution Board/Backplane	IDSEL	Interrupt Pin on Device	Interrupt Pin on PCI-Bridge
1	AD21	INTA# INTB# INTC# INTD#	IRQX IRQY IRQZ IRQW
2	AD22	INTA# INTB# INTC# INTD#	IRQY IRQZ IRQW IRQX
3	AD23	INTA# INTB# INTC# INTD#	IRQZ IRQW IRQX IRQY

5.1.3 Onboard resources

The onboard devices of your SOM 144 Module need IRQ and DMA resources.

PCI 2.1 specifications allow resources to be shared by multiple devices.

If you use a non PCI 2.1 compliant devices it is strictly recommended to consult your SOM 144 manual or your SOM 144 supplier.

Please ask your supplier of the external PCI devices for PCI 2.1 compatibility. It's recommended for backplane designers to integrate the PCI devices on the specific backplane from device 0 upward.

5.2 Power supply definition

Total number of power supply pins:

Current rating per pin: 0.3A at SODIMM , 0.4A at the recommended front-end connector.

The SOM 144 Module's power pins can not be used to supply power to I/O Boards. The I/O slots' power must be supplied by the solution board of the SOM 144 Module.

Pin numbers	SODIMM socket	Recommended connector
GND	12	14
VCC	9	0
12V	0	1
5VSB	0	3

5.3 Electrical Specifications

Supply voltage: $5V_{DC}$ +/- 5%

Supply voltage ripple: 100 mV peak to peak 0 – 20 MHz

5.4 Serial ports

All Serial ports drive with TTL outputs. All ports are 16550 compatible with 16 byte send/receive FIFO or better.

Maximum baud rate up to 115k bps is supported. Please ask your SOM 144 Module supplier for higher baud-rates.

5.5 IrDA

SOM 144 supports consumer IR, IrDA version 1.0 SIR (115kbps) and version 1.1 MIR(1.152Mbps) and FIR(4MBbps).

5.6 Parallel Port

The parallel port is compatible with IBM parallel port, SSP. For support of PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP) please ask your SOM 144 Module supplier.

Also for extension FDD port support on printer port signals contact your SOM 144 Module supplier.

5.7 FDD

SOM 144 Modules don't support a standard floppy interface. It's recommended for the SOM 144 Module designer to support a extension FDD port support on printer port signals. Please ask your SOM 144 Module supplier for this.

5.8 IDE

All SOM 144 Modules supports up to 2 IDE devices and DMA33 mode. UDMA66 and faster needs additional signals and is not supported by the SOM 144 standard. Please ask your SOM 144 Module supplier for further details.

5.9 Ethernet specification

A SOM 144 Module needs an external transformer on the

solution board for 10/100 BaseT support, such as Pulse H1102 or others take following specifications of Ethernet transformer:

Tx turns ratio: 1:1 +/- 5%

Rx turns ratio: 1:1 +/- 5%

Insertion Loss 100KHz to 100MHz: -1.1 dB Max

Return Loss 1 to 80 MHz: -10 dB Max

Differential to Common Mode Rejection,
1 to 80 MHz: -30 dB Min

Cross Talk 1 to 80 MHz: max. 35 dB

Hi-Pot (Pri-Sec): min. 1500VRMS

APPENDIX A

LITERATURE, STANDARDS, LINKS

This SOM 144 specification and design guide does not cover information regarding standard PC technology. Please refer to this selection of different information sources for your convenience.

A.1 Standard PS/2 - Connectors

- AT BUS Design IEEE P996 Compatible, **Edward Solari, Annabooks San Diego CA. ISBN 0-929392-08-6**
- PC Handbook, Sixth Edition, **John P. Choisser and John O. Foster, Annabooks San Diego CA. ISBN 0-929392-36-1**
- AT IBM Technical Reference Vol. 1&2, **1985**
- Personal Computer Bus Standard P996, **Draft D2.00, January 18, 1990, IEEE Inc**
- ePanorama PC Hardware Linkpage

A.2 RS232C

- EIA-232-E Interface between data terminal equipment and date circuit-terminating equipment employing serial binary data interchange (ANSI/IEA-232-D)

National Semiconductor's Interface Data Book includes any applications notes. These notes are also available online at http://www.national.com/. A search engine is provided to search the text of the available application notes. Entering „232" as search criteria to get a current list of related application notes.

A.3 ATA

The ATA specification of X3T10 is available from several ftp servers.

Please search for „ata3-r6" on ftp search engines.

It's highly recommended to have a view on "4..2 I/O cable" in this specification by using harddisks on DMA33 or PIO4-Mode.

A.4 USB

The USB specification maybe obtained from the USB Implementers Forum web site at www.usb.org

A.5 PCI

The PCI local bus specification maybe obtained from the PCI Special Interest Group web site at http://www.pcisig.com/.

A.6 ATX

The ATX specification maybe obtained from the Intel website.

Please go to http://developer.intel.com/ and make quick search for ATX specification. Some other documents are available on http://www.teleport.com/~ffsupprt/.

A.7 AC-LINK 97 (AC97)

The SOM 144's AC97 interfaces is compliant with AC97 Specification Revision 1.3, 2.0, and 2.1. For Revision 2.1 specification, plese refer ftp://download.intel.com/ial/scalableplatforms/audio/ac97r21.pdf